IN THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Currently Amended) A computer system comprising:

a processor for controlling operations of the computer system;

a bus coupled to the processor; and

an interface device, coupled to the processor through the bus, comprising:

a first controller for performing a first logic operation; and

a second controller coupled to the first controller for performing a second logic operation;

wherein when the processor initializes the ~~apparatus~~ interface device, the first controller responds with a message to the processor to indicate that the ~~apparatus~~ interface device is a single-function device and the second controller is disabled,

wherein the first controller determines which one of the first controller and the second controller responds to the processor according to a command from the processor.

2. (Currently Amended) The computer system of claim 1, wherein the interface device comprises:

a selecting module coupled to the second controllers for allowing either the first controller or the second controller to utilize the bus[[;]]

3. (Original) The computer system of claim 1, wherein the first controller comprises:

a register for storing a flag used to control whether either the first controller or the second controller is enabled.

4. (Original) The computer system of claim 1, wherein the interface device is a PCI interface device and the bus is a PCI bus.

5. (Original) The computer system of claim 1, wherein when the processor initializes the interface device, the first controller responds with a message to the processor to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller.

6. (Currently Amended) The computer system of claim 1, wherein the interface device further comprises:

a third controller coupled to the first controller for performing a third logic operation.[[;]]

7. (Currently Amended) The computer system of claim 1, wherein the interface device further comprises:

a third controller coupled to the second controller for performing a third logic operation.[[;]]

8. (Original) An apparatus coupled to a processor through a bus, the apparatus comprising:

a first controller for performing a first logic operation, wherein when the processor initializes the apparatus, the first controller responds with a message to the processor to indicate that the apparatus is a single-function device; and

a second controller coupled to the first controller for performing a second logic operation, wherein when the processor initializes the apparatus, the second controller is disabled;

wherein the first controller determines which one of the first controller and the second controller responds to the processor according to a command from the processor.

9. (Currently Amended) The apparatus of claim 8, further comprises:
a selecting module coupled to the first and second controllers for allowing either the first controller or the second controller to utilize the bus.[[;]]

10. (Original) The apparatus of claim 9, wherein the selecting module is within the first controller.

11. (Original) The apparatus of claim 9, wherein the first controller comprises:
a register for storing a flag used to control the operation of the selecting module.

12. (Original) The apparatus of claim 8, wherein the first controller comprises:
a register for storing a flag used to control whether either the first controller or the second controller responds to the processor.

13. (Original) The apparatus of claim 12, wherein the flag is changed by the processor.

14. (Currently Amended) The apparatus of claim 9, wherein the bus is a PCI bus and the first controller further comprises:
a first INTB pin, a first REQB pin, a first GNTB pin, and a first IDSEL pin, all coupled to the PCI bus.

15. (Original) The apparatus of claim 14, wherein each of the controllers further comprises:
at least a plurality of address pins, a Frameb pin, an Irdyb pin, and a Trdyb pin, all coupled to the selecting module, wherein the address pins, the Frameb pin, the Irdyb pin, and the Trdyb pin are in accordance with the PCI specification.

16. (Original) The apparatus of claim 8 wherein when the processor initializes the

apparatus, the first controller responds with a message to the processor to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller.

17. (Original) A method for using a bus in the computer system which comprises a processor and an interface device, the interface device comprising a first controller and a second controller, and being coupled to the processor through the bus, the method comprising:

generating a first message to indicate that the interface device is a single-function device when the interface device is initialized;

generating a second message to request a total memory volume including a first portion that will be utilized by the first controller and a second portion that will be utilized by the second controller; and

determining which one of the first controller and the second controller responds to the processor according to a command from the processor.

18. (Original) The method of claim 17 further comprising:

using a flag stored in a register of the first controller to control whether either the first controller or the second controller responds to the command.

19. (Original) The method of claim 18 wherein the flag is changed by the processor.

20. (Original) The method of claim 18 wherein further comprising:

disabling the second controller when the interface device is initialized.